

What is claimed is:

1. A method of fabricating a metal layer in an integrated circuit, the method comprising the steps of:
  - 5 depositing a layer of metal alloy which contains alloy dopant precipitates;
  - performing a first anneal of the integrated circuit to drive the alloy dopants into solid solution;
  - quenching the integrated circuit to prevent the alloy dopants from coming out of solution;
  - 10 removing excess metal alloy using a polish process;
  - performing a second anneal after the excess metal alloy is removed to allow the dopants to come out of solution and increase a conductivity of the metal alloy.
2. The method of claim 1 wherein the first anneal is performed at 400 to 500° C.
3. The method of claim 1 wherein the metal alloy comprises aluminum with alloy dopants of silicon and copper.
4. The method of claim 1 wherein the second anneal is performed at 150 to 250° C.
5. The method of claim 1 further comprising the steps of:
  - forming vias and interconnect trenches in the integrated circuit prior to
  - 25 depositing the layer of metal alloy; and
  - wherein the polish process removes excess metal alloy to define metal interconnect lines.

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6. A method of fabricating a metal layer in an integrated circuit, the method comprising the steps of:
- forming vias and interconnect trenches in the integrated circuit;
  - depositing a layer of metal alloy which contains alloy dopant precipitates on the integrated circuit to fill the vias and interconnect trenches;
  - performing a first anneal of the integrated circuit at 400 to 500° C to drive the alloy dopants into solid solution;
  - quenching the integrated circuit to prevent the alloy dopants from coming out of solution;
  - removing excess metal alloy using a chemical-mechanical polish process;
  - performing a second anneal at 150 to 250° C after the excess metal alloy is removed to allow the dopants to come out of solution and increase a conductivity of the metal alloy.
7. The method of claim 6 wherein the metal alloy comprises aluminum with alloy dopants of silicon and copper.
8. Method of improving a chemical-mechanical polish (CMP) process in an integrated circuit, the method comprises the step of annealing the integrated circuit prior to performing the chemical-mechanical polish process to drive alloy dopants into solid solution.
9. The method of claim 8 wherein the anneal is performed at approximately 400 to 500° C.
10. The method of claim 8 wherein the method further comprises annealing the integrated circuit after performing the chemical-mechanical polish process to drive alloy dopants out of solid solution.

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metal contacts and interconnects coupled to the memory array and internal circuitry, wherein the metal contacts and interconnects are formed by annealing the memory at a temperature sufficient to drive alloy dopants into solid solution prior to polishing the memory device to remove portions of a metal layer and form the metal contacts and interconnects.

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19. The memory device of claim 18 wherein the memory device is annealed following the polishing the memory device to increase a conductivity of the metal contacts and interconnects.

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